What is Claimed is:

1. A tape carrier for a semiconductor device comprising a flexible insulation tape having via holes for a solder ball, a metal wiring layer formed on one surface of the insulation tape, the via halls for the solder balls having an opening on the other surface of the insulating tape, and a ring-shaped metal brace formed on the periphery of the opening of the respective via holes and provided with a cutout opening having a width up to 4 % of the circumferential length of the periphery.

2. A tape carrier for a semiconductor device comprising a flexible insulation tape having via holes for a solder ball, a metal wiring layer formed on one surface of the insulation tape, the via halls for the solder balls having an opening on the other surface of the insulating tape, and a metal brace formed on the periphery of the opening of the respective via holes and comprising a plurality of arcuate shape portions, such that gaps are simetorically provided and positioned between the arcuate shape portions,, and that the total width of the gaps is up to 40% of the circumferential length of the periphery.

3. A tape carrier for a semiconductor device of ~~one of Claims 1 and 2~~ Claim 1, wherein the metal braces have a surface to which Ni plating is applied, and Au plating is applied to the Ni plating.

4. A tape carrier for a semiconductor device of ~~one of Claims 1 and 2,~~ Claim 1

wherein the metal braces have a surface to which Au plating is applied.

5. A method for manufacturing a tape carrier for a semiconductor device comprising the steps of forming a metal foil on both surfaces of the flexible insulation tape, forming a metal wiring layer for mounting semiconductor chips on one face by forming a protective film and then etching and removing the protective film, exposing the insulation tape at desired positions on the other face, protecting one of the surfaces including the metal wiring layer by a protective film of resin, forming via holes by performing etching on the exposed portion of the insulation tape at the desired positions, forming a resin protective film on the via holes and part of the periphery of the via holes, and removing said metal foil at the portion exposed from the protective film by etching, wherein a width of the removed metal foil at the periphery of the opening of the via halls is up to 4 % of the circumferential length of the periphery, and the remaining portion of the metal foil forms a ring-shaped metal brace, and then removing the protective film formed on both surfaces of the insulation tape.

6. A method for manufacturing a tape carrier for a semiconductor device comprising the steps of forming a metal foil on both surfaces of the flexible insulation tape, forming a metal wiring layer for mounting semiconductor chips

on one face by forming a protective film and then etching and removing the protective film, exposing the insulation tape at desired positions on the other face, protecting one of the surfaces including the metal wiring layer by a protective film of resin, forming via holes by performing etching on the exposed portion of the insulation tape at the desired positions, forming a resin protective film on the via holes and a plurality of portions of the periphery of the via holes, and removing said metal foil at the portion exposed from the protective film by etching, such that the remaining portion of the metal foil forms a metal brace, and then removing the protective film formed on both surfaces of the insulation tape, whereby the metal brace comprises a plurality of arcuate shape portions, such that gaps are simetorically provided and positioned between the arcuate shape portions, and that the total width of the gaps is up to 40 % of the circumferential length of the periphery.

7. A method of ~~one of Claims 5 and 6,~~ Claim 5 wherein the metal braces have a surface to which Ni plating is applied, and Au plating is applied to the Ni plating.

8. A method of ~~one of Claims 5 and 6,~~ Claim 5 wherein the metal braces have a surface to which Au plating is applied.

9. A semiconductor device using the tape carrier for the semiconductor device of ~~one of Claims 1 to 4~~ Claim 1, wherein semiconductor chips are connected to the metal wiring layer, and the solder balls are mounted so as to cover the via holes and the metal braces, such that the metal wiring layer is electrically connected to the solder balls.

10. A method of manufacturing a semiconductor device comprising the steps in ~~one of Claims 1 to 4~~ Claim 1, and further the steps of connecting semiconductor chips to the metal wiring layer, and mounting solder balls to cover the via holes and the metal braces, and electrically connected the metal wiring layer to the solder balls.

11. A tape carrier for a semiconductor device comprising a flexible insulation tape for mounting semiconductor chips and having via holes there through at desired locations, a metal wiring layer formed on one surface of the insulation tape and electrically connected to the semiconductor chips, solder balls formed on the other surface of the insulating tape and electrically connected to the metal wiring layer through the via halls, and a ring-shaped metal brace formed on the other surface of the insulation tape at a location of the respective solder balls in contact with the solder balls and provided with a cutout opening having a width up to 4 % of the circumferential length of the periphery.

12. A tape carrier for a semiconductor device comprising a flexible insulation tape for mounting semiconductor chips and having via holes there through at desired locations, a metal wiring layer formed on one surface of the insulation tape and electrically connected to the semiconductor chips, solder balls formed on the other surface of the insulating tape and electrically connected to the metal wiring layer through the via halls, and a metal brace formed on the other surface of the insulation tape at a location of the respective solder balls in contact with the solder balls and comprising a plurality of arcuate shape portions, such that gaps are simetorically provided and positioned between the arcuate shape portions,, and that the total width of the gaps is up to 40 % of the circumferential length of the periphery.